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SEMICONDUCTOR LASER JOINT STUDY PROGRAM WITH ROME LABORATORY

Cornell University

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13. ABSTRACT (Maximum 200 words)

A program to jointly study vertical-cavity surface emitting lasers (VCSEL) for high speed vertical optical interconnects (VOI) has been conducted under an ES&E between Rome Laboratory and Cornell University. Lasers were designed, grown, and fabricated at Cornell University. A VCSEL measurement laboratory has been designed, built, and utilized at Rome Laboratory. High quality VCSEL material was grown and characterized by fabricating conventional lateral cavity lasers that emitted at the design wavelength of 1.04um. The VCSELs emit at 1.06um. Threshold currents of 16 mA at 4.8 volts were obtained for 30um diameter devices. Output powers of 5 mW were measured. This is 500 times higher power than from the light emitting diodes employed previously for vertical optical interconnects. A new form of compositional grading using a cosinusoidal function has been developed and is very successful for reducing diode series resistance for high speed interconnection applications. A flip-chip diamond package compatible with high speed operation of 16 VCSEL elements has been designed and characterized. A flip-chip device binding effort at Rome Laboratory was also designed and initiated. This report presents details of the one-year effort, including process recipes and results.

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1) Abstract

A program to jointly study vertical-cavity surface emitting lasers (VCSEL) for high speed vertical optical interconnects (VOI) has been conducted under an ES&E between Rome Laboratories and Cornell University. Lasers were designed, grown and fabricated at Cornell University. A VCSEL measurement laboratory has been designed, built and utilized at Rome Laboratory. High quality VCSEL material was grown and characterized by fabricating conventional lateral cavity lasers which emitted at the design wavelength of 1.04μm. The VCSELs emit at 1.06μm. Threshold currents of 16 mA at 4.8 volts were obtained for 30μm diameter devices. Output powers of 5 mW were measured. This is 500 times higher power than from the light emitting diodes employed previously for vertical optical interconnects.

A new form of compositional grading using a cosinusoidal function has been developed and is very successful for reducing diode series resistance for high speed interconnection applications. A flip-chip diamond package compatible with high speed operation of 16 VCSEL elements has been designed and characterized. A flip-chip device bonding effort at Rome Labs was also designed and initiated. This report presents details of the one year effort, including process recipes and results.

2) Discussion

Optical interconnects and optical computing require fast light source that dissipate small amounts of power and occupy small size. The semiconductor laser is the most likely candidate for these requirements. The approach in this study uses vertical-cavity surface-emitting lasers (VCSEL)s for greatest packing density and addressable array format. Two key issues in using the VCSEL for high speed optical interconnects are power dissipation (heating) and electrical connections with low parasitic losses. Toward reducing heat dissipation, graded interfaces in the AlGaAs/AlGaAs mirror layers are required to remove valence band discontinuities which contribute significant series resistance which results in resistive heating. To better remove diode heat, a diamond heat sink has been designed for high speed flip-chip connections to the VCSEL. High speed transmission lines on diamond have been demonstrated in this study.

Packaging these diode arrays is the final assembly step prior to testing. The design of the package was completed prior to the design of the VCSEL layer structure and process. In this study, flip-chip mounting was selected for the best possible heat removal from the VCSELs. The distance from the source of diode heat to the heat sink was thus minimized. Diamond was selected for high thermal conductivity. VCSELs can be designed to emit out of the top, or out of the bottom of the structure. The use of flip-chip geometries required design of the VCSEL with laser emission through the substrate side (bottom). The VCSEL mirrors were designed with substrate-side emission and compatibility with packaging solders as a goal.

2.1 Background

Vertical-cavity surface-emitting lasers are attractive candidates for optical interconnects because of high packing density with narrow optical beams[1] and low

[1]J.L. Jewell, A. Scherer, S.L. McCall,Y.H. Lee, S. Walker, J.P. Harbison, and L.T. Florez, "Low threshold electrically pumped vertical-cavity surface emitting microlasers," *Electron. Lett.*, vol. **25** pp. 1213-1124, 1989.

threshold currents[2]. The round geometry of the devices produces circular radiation patterns[3] which are superior for fiber coupling over lateral lasers. The circular beam can also be better suited for vertical optical interconnections. The circular beam is much more compact than the LEDs used in previous vertical optical interconnect studies[4] Higher packing density can result from the narrower beam diameter. The small size also facilitates 2-D addressable array fabrication for parallel communications.

VCSEL arrays have been extended beyond parallel sources at a single wavelength to sources at different wavelength for each emitting element[5]. Operation to 5 Gb/s have been shown for this configuration[6]. It is estimated that an array of these devices could be combined to reach terabit per second transmission rates.

The VCSEL gain region volume is very small , therefore very high reflectivity mirrors are required for lasing. Multilayer stacks of AlGaAs layers of different compositions can provide a very high reflectivity over a very narrow wavelength passband. The gain region and mirror reflectivities must match very closely in wavelength.

An undesirable consequence of using AlGaAs mirror stacks is the conduction and valence band offsets between the mirror materials. These offsets can contribute significant series resistance to the VCSEL diode by acting as barriers to carriers

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[2]R.S. Geels, S.W. Corzinne, J.W. Scott, D.B. Young, and L.A. Coldren, "Low threshold planarized vertical cavity surface emitting lasers", *IEEE Photon. Technol. Lett.*, vol. **2**, pp. 234-236, 1990.

[3]C.J. Chang-Hasnain, M. Orenstein, A. Von Lehmen, L.T. Florez, J.P. Harbison, and N.G. Stoffel, "Transverse mode characteristics of vertical-cavity surface-emitting lasers," *Appl. Phys. Lett.*, vol. 57, pp. 218-219, 1990.

[4]H.F. Bare, F. Haas, D.A. Honey, D. Mikolas, H.G. Craighead, G. Pugh and R. Soave, "A simple Surface-Emitting LED Array useful for developing Free-Space Optical Interconects," *IEEE Phot. Tech. Let.*, Vol. **5**, No. 2, p. 172-175, February 1993.

[5]C.J. Chang-Hasnain, J.P. Harbison, C-E. Zah, M.W. Maeda, L.T. Florez, N.G. Stoffel and T-P. Lee, "Multiple Wavelength Tunable Surface-Emitting Laser Arrays," *IEEE J. of Quantum Elec.*, vol 27., pp.1368-1376, 1991.

[6]M..W. Maeda, C. Chang-Hasnain, A. Von Lehman, H. Izadpanah, C. Lin, M.Z. Iqbal, L.Florez, and J. Harbison, "Multigigabit/s operation of 16-wavelength vertical-cavity surface-emitting laser array," *IEEE Photonics Tech. Lett.*, vol. **3**, pp. 863-865, 1991.

which must be overcome by applying additional bias to the diodes. Fortunately the electrons can effectively tunnel through the barriers. Holes, which have heavier effective mass, cannot tunnel through the barriers, thus the p-type mirror contributes the majority of the diode series resistance.

The requirement for substrate side emission dictates that the laser must emit at a wavelength longer than 880nm, the band-edge of the GaAs substrate. For this study, strained layer quantum wells made from GaInAs were chosen to provide emission at 1040nm to meet this requirement. These strained quantum wells also have the advantage of reduced threshold currents as a result of strain modifications to the structure of the valence band[7].

3 Design and Fabrication

3.1 Mirror Design

The VCSEL design for substrate side emission established one of the requirements for wafer structure. Mirrors must be designed to produce lasing in the desired direction. The starting point for this design was to utilize a program[8] that would model the structure of the mirrors to be used in this device. The program uses a numerical technique called a scattering matrix approach. Using known boundary conditions, such as the GaAs/air top mirror interface and the AlGaAs/substrate bottom interface, an electromagnetic wave is propagated through the structure taking into account all interfaces and the wavelength dependent dielectric constants of all materials[9]. This program is resident on a VAX 4000-200 running VMS and managed by Dr. W. Schaff at Cornell University. Some Photonics Center staff have accounts there via on-site terminals, or remote Internet access using TELNET or RLOGIN. Calculated reflectivity as a function of wavelength is seen in Figure 1.

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[7]W.J. Schaff, P.J. Tasker, M.C. Foisy and L.F. Eastman, "Device Applications of Strained layer Epitaxy", Vol. **33**, Semiconductors and Semimetals, T.Pearsll Ed.,Academic Press, New York, 1992.

[8]FORTRAN program XALGRD developed under ONR AASERT Grant Number N00014-89-J-1386

[9]D.W. Jenkins, "Optical constants of $Al_xGa_{1-x}As$," J. *Appl. Phys.* vol. **68** (4), P. 1848-1853, Aug. 1990.

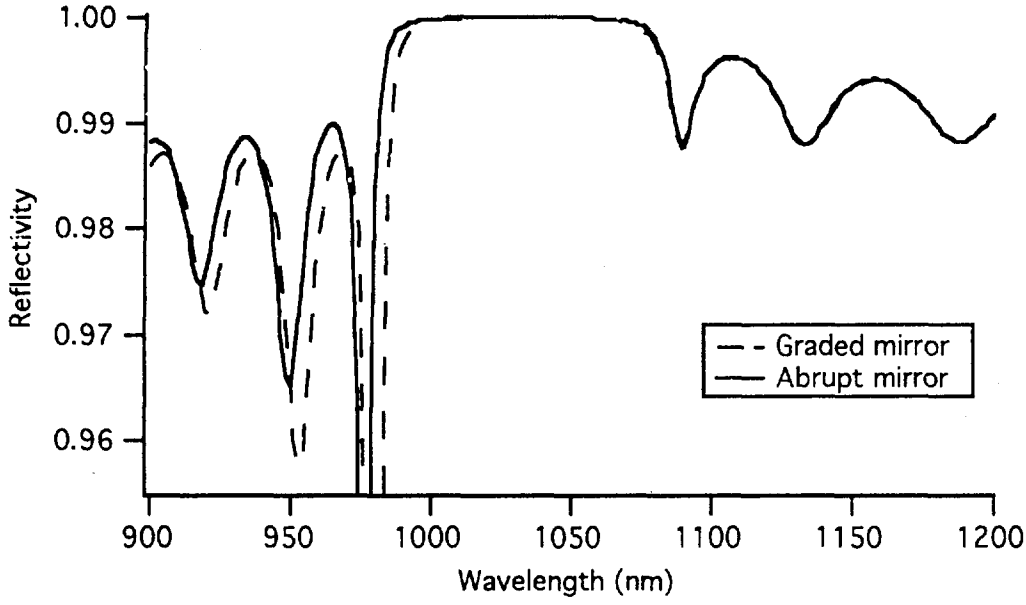


Figure 1 Calculated reflectivity as a function of wavelength for the abrupt and the graded interface mirror designs

3.2 Wafer Design

The layer designs use the AlGaAs/AlGaAs mirrors described above for bottom side emission, and strained GaInAs quantum wells for emission at 1040nm. Two designs were studied. The first design used abrupt interfaces between the mirror stack layers and the second design had graded interfaces. The abrupt interface design was used to confirm agreement between theoretical predictions of mirror reflectivity and experimental results. The cosine compositional grading between mirror layers could then be compared to a reference for optical reflectivity and electrical resistance behavior.

Function	Al (or In)%	Abrupt (Å)	Graded (Å)
p+ cap	0%	1462.4	639.2
Low Al	10%		557.5
Graded	10%->90%		200
High Al	90%	857.4	641.8
Graded	90%->10%		200
Low Al	10%	744.8	557.5
Graded	90%->10%		200
High Al	90%	857.4	641.8
Graded	10%->90%		200
Barrier	0%	1247.4	1155.3
QWell	30% (In)	50	50
Barrier	0%	140	140
QWell	30% (In)	50	50
Barrier	0%	140	140
QWell	30% (In)	50	50
Barrier	0%	140	140
Barrier	0%	1247.4	1155.3
Graded	10%->90%		200
High Al (90%)	90%	857.4	641.8
Graded	90%->10%		200
Low Al (10%)	10%	744.8	557.5
Graded	10%->90%		200
High Al (90%)	90%	857.4	641.76
Graded	90%->10%		200
n+buffer	0%	~3000	~3000
SI substrate			

Table I Dimensions and compositions of abrupt and graded interface VCSELs

3.3 Laser Wafer Growth by Molecular Beam Epitaxy

The VCSEL structures were grown by molecular beam epitaxy (MBE) at Cornell. In Figure 2 the growth sequence for the abrupt interface VCSEL entered by the operator is seen. The structure is input as growth rate and doping concentration. The growth rates of the Group III elements establish thicknesses and compositions. Translation of growth rates and doping concentrations into furnace temperatures occurs at the time of growth using calibrations derived from least square fits to lookup tables of rates or concentration and temperatures which have been established just prior to growth.

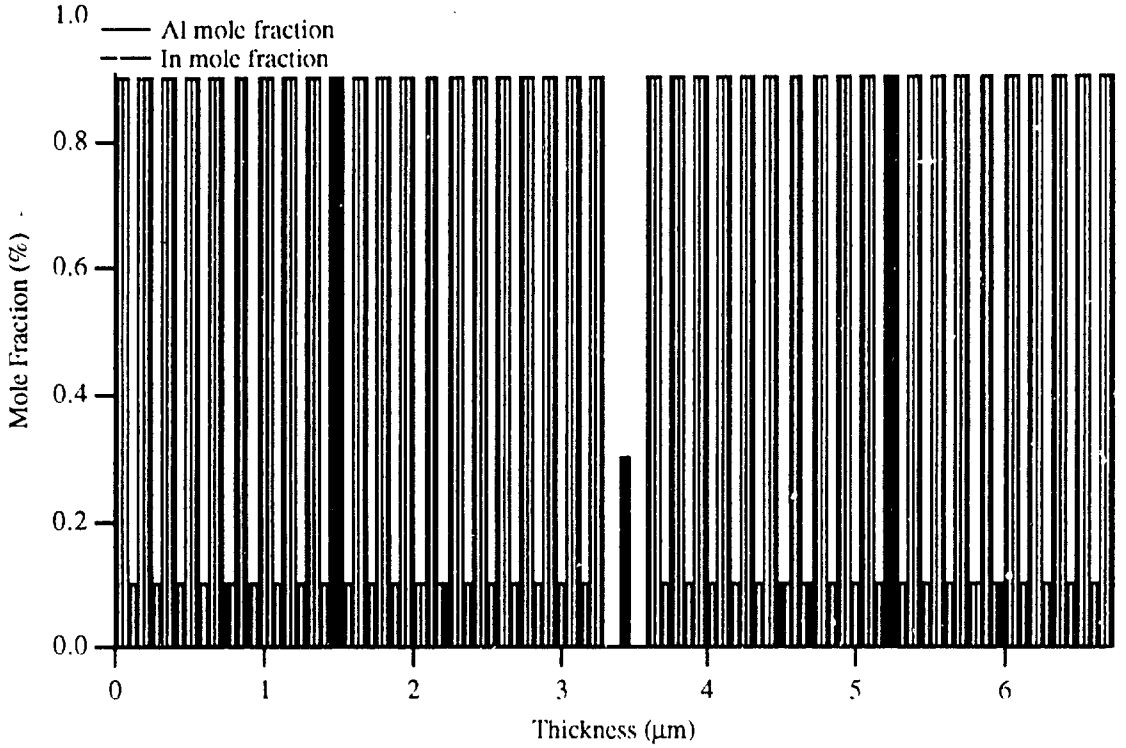


Figure 2 Alloy compositions for the abrupt interface mirror VCSELs

A plot of furnace temperatures versus time required for the structure of Figure 2 is seen in Figures 4 and 5. It can be seen that the Ga and Al temperatures are changed to provide different mole fractions in the mirrors. The substrate temperature is selected for optimized quality for each material. The mirrors are grown at a substrate temperature of 620°C to avoid any desorption of Ga which would occur at temperatures greater than 640°C. It would be desirable to grow AlGaAs layers at

higher substrate temperatures for higher quality material, but the thicknesses and compositions would then become a function of substrate temperature. Substrate temperature reproducibility and accuracy are not sufficient in most MBE systems to avoid uncertain amounts of variation of Ga desorption. A compromise in the design of the VCSEL mirrors is to insert thin (<10Å) GaAs layers into any thick AlGaAs layer grown at 620°C[10]. The thin GaAs layer serves to smooth the growth front of AlGaAs which will become atomically rough with increasing AlGaAs thickness[11].

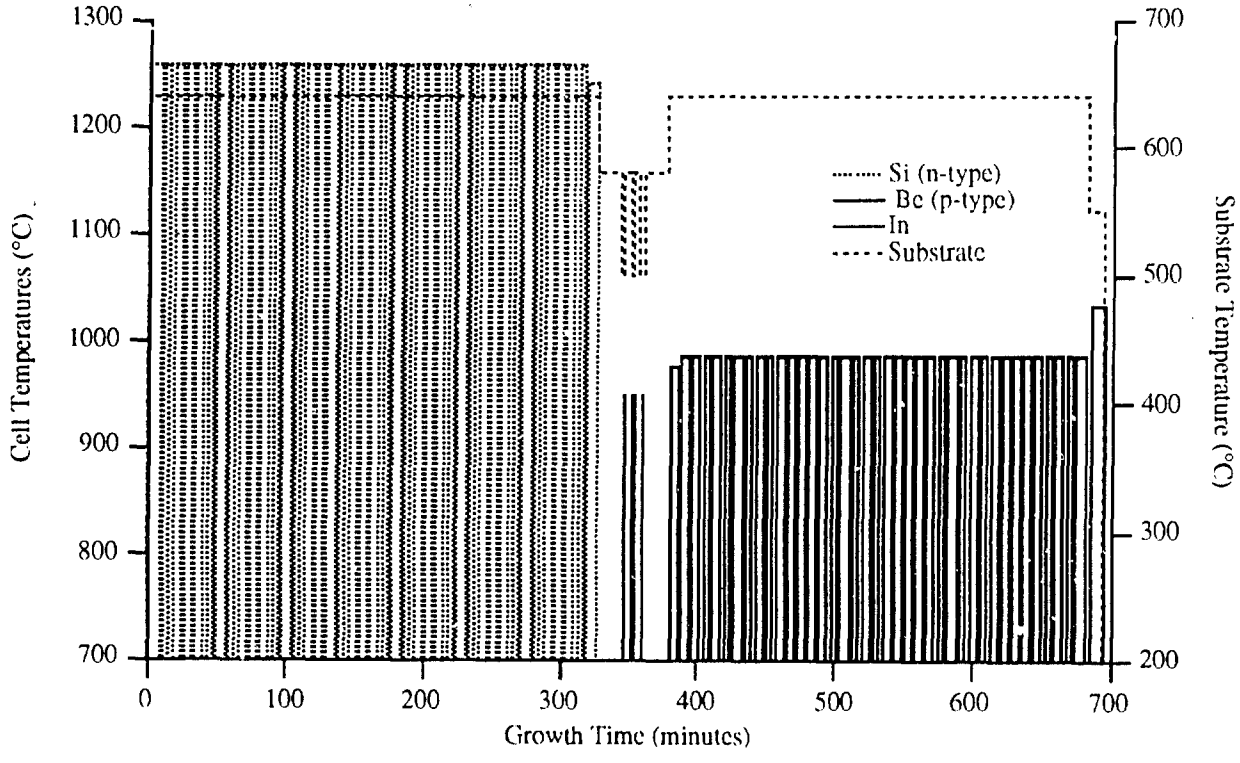


Figure 3 Dopant, In and substrate temperatures versus time for the abrupt interface VCSEL

[10]S.D. Offsey, W.J. Schaff, P.J. Tasker, H. Ennen, and L.F. Eastman, "Strained-Layer InGaAs-GaAs-AlGaAs Graded-Index Separate-Confinement Heterostructure Single Quantum Well Lasers Grown by Molecular Beam Epitaxy," *Appl. Phys. Lett.*, **54** (25), p. 2527-2529 (June 19, 1989).

[11]W.J. Schaff, L.F. Eastman, B. Van Rees, and B. Liles, "Superlattice Buffers for GaAs Power MESFETs Grown by MBE," *5th MBE Workshop*, Atlanta, Ga (Oct. 6-7, 1983); *J. Vac. Sci. Tech.*, **B2** (2), 265-268 (Apr.-June 1984).

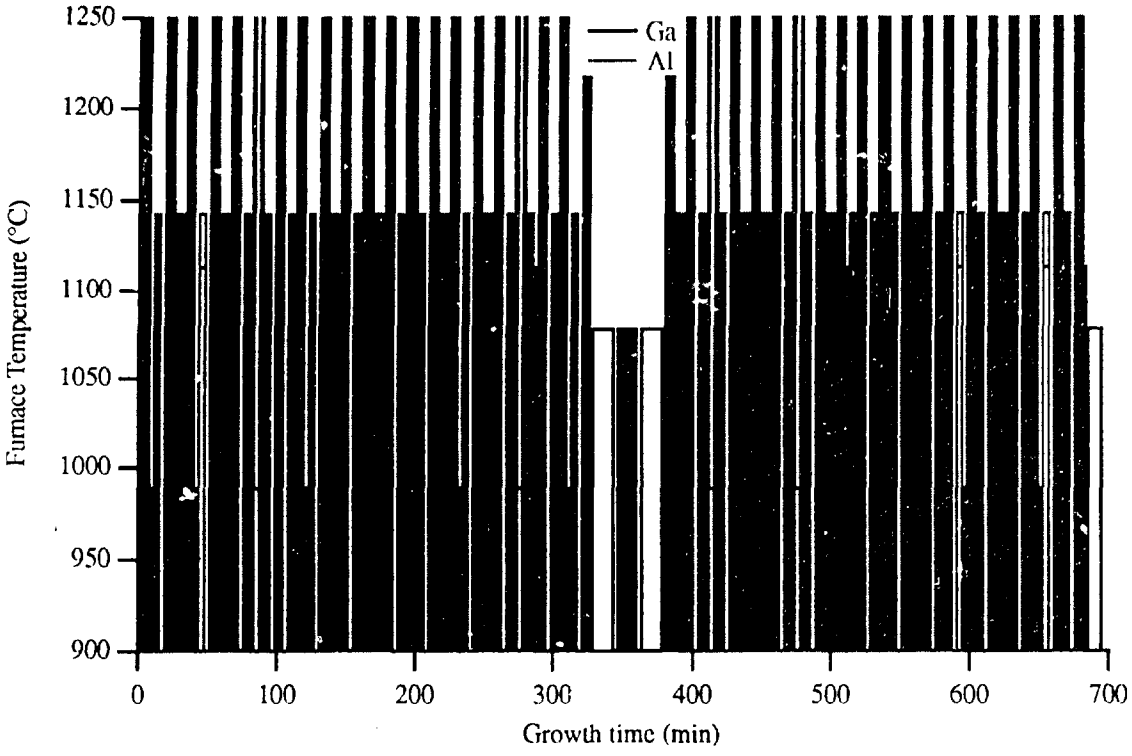


Figure 4 Ga and Al temperatures versus time for the abrupt interface mirror VCSELs

GaAs surrounding the quantum wells is grown at 580°C while the strained GaInAs quantum wells are grown at 500°C. Desorption of In from GaInAs will occur at temperatures higher than 520°C[12]. A 20°C margin is employed to prevent uncertainties in In mole fraction and quantum well thickness as a result of desorption.

In Figure 5 the structure for the cosinusoidally graded composition interface mirror VCSEL entered by the operator is shown. Within the limit of resolution seen in this figure, it is not possible to detect much difference by eye between this structure and the abrupt interface VCSEL. The corresponding temperature versus time plots seen

[12]"MBE Growth and Material and Device Characterization of Strained GaInAs Grown on GaAs for Application to MODFETs", W.J. Schaff and L.F. Eastman, *Proc. E-MRS*, Vol. **XVI**, 295-301 Strasbourg, France (June 2-5, 1987).

are Figure 6 are also quite similar at this resolution to the abrupt interface VCSEL. Expanded views of the Al temperature versus time for the graded interface mirror VCSELs is shown in Figure 7. The temperature changes required for cosinusoidally changing composition with distance are shown. Extensive computer control of the MBE facilities developed previously at Cornell[13] is required to permit growth of these complex profiles.

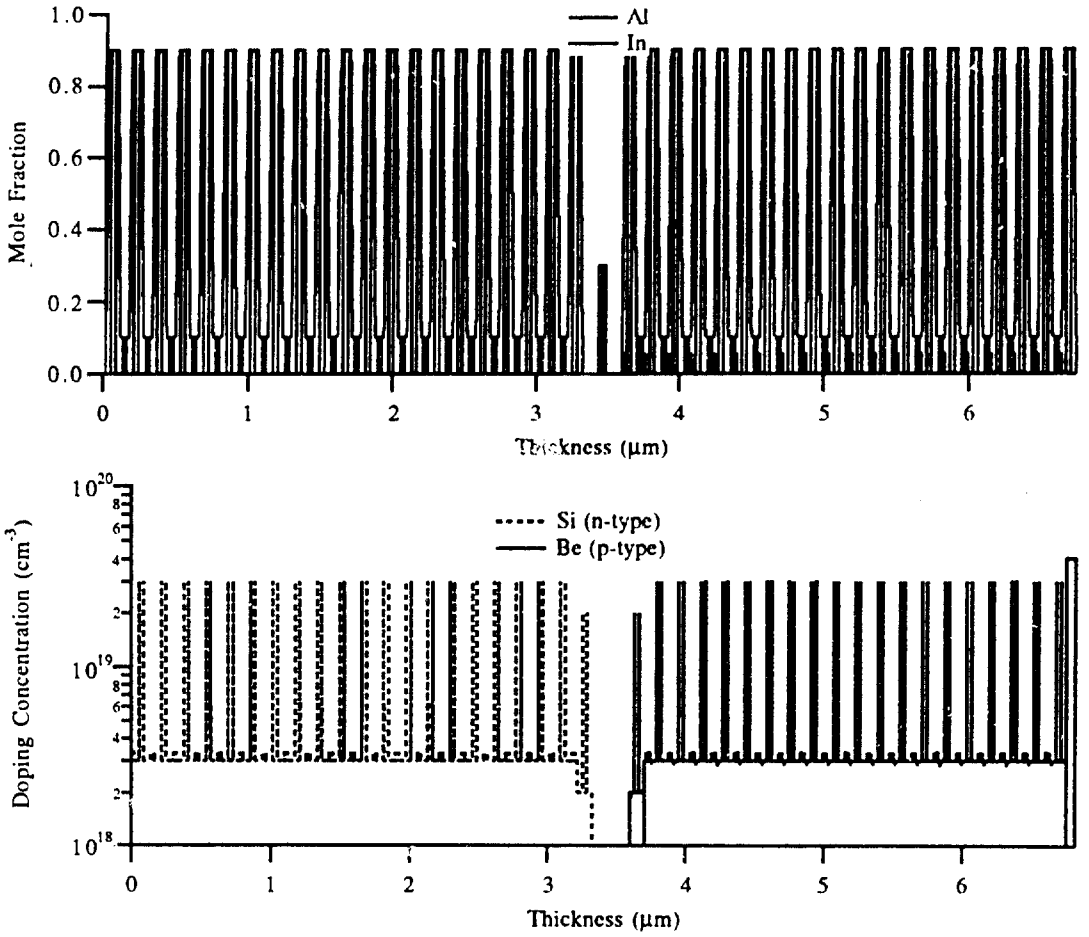


Figure 5 Compositions and doping for the graded interface mirror VCSELs

Obtaining the desired composition profile required that Ga and Al furnace temperatures closely follow the temperature curves shown. This is not possible for high growth rates because the furnace temperature is required to change by large

[13]W.J. Schaff, PhD thesis, 1984, Cornell University, Ithaca, NY

amounts in small times. Although control signals could be sent to the furnace requesting these large changes, there would be a thermal lag between setpoint and actual temperature at the onset of these changes, and possible temperature overshoot at the end of a series of temperature changes.

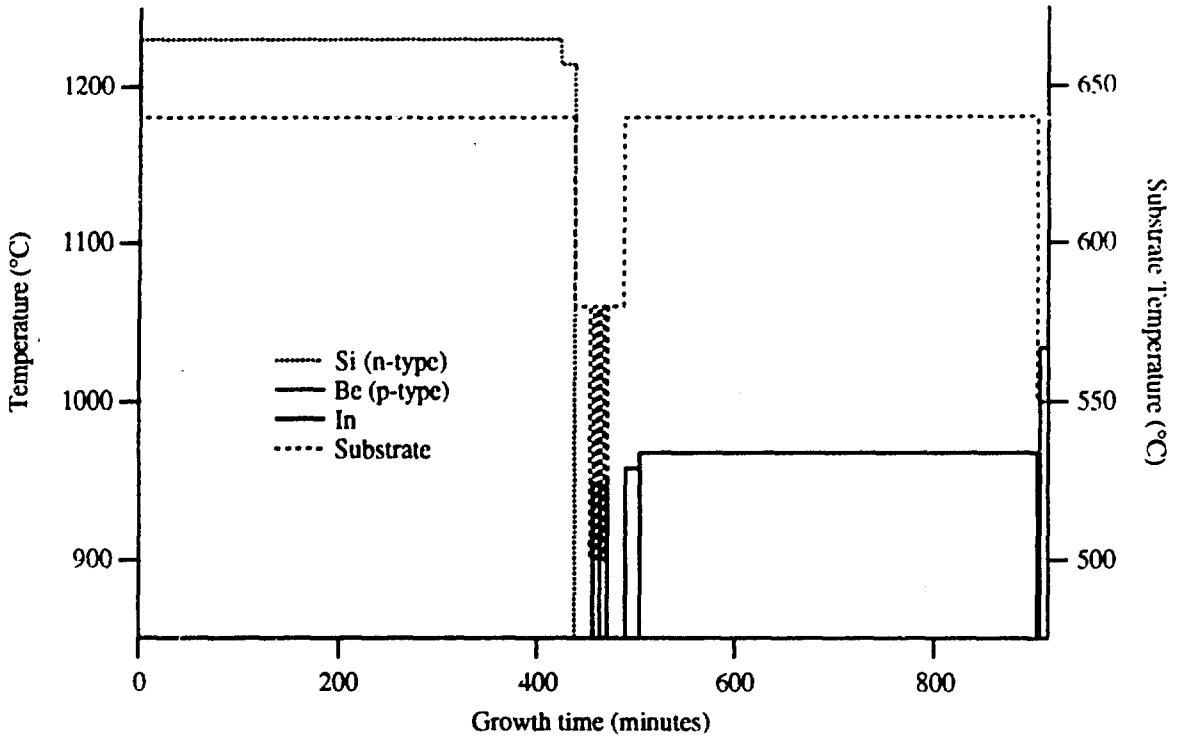


Figure 6 MBE furnace and substrate temperatures for the cosinusoidally graded interface mirror VCSELs. The substrate temperature is lowered to 580 C for GaAs and 500 C for strained GaInAs quantum well growth. The dopant temperatures can be kept constant for uniform doping concentration because the growth rate is held constant.

Uncontrolled deviation from required profiles translates into composition changes with distance which do not meet requirements for high mirror reflectivity. These problems are avoided by keeping the temperature changes small enough to keep the furnace in relatively close thermal equilibrium with the desired temperature/time changes.

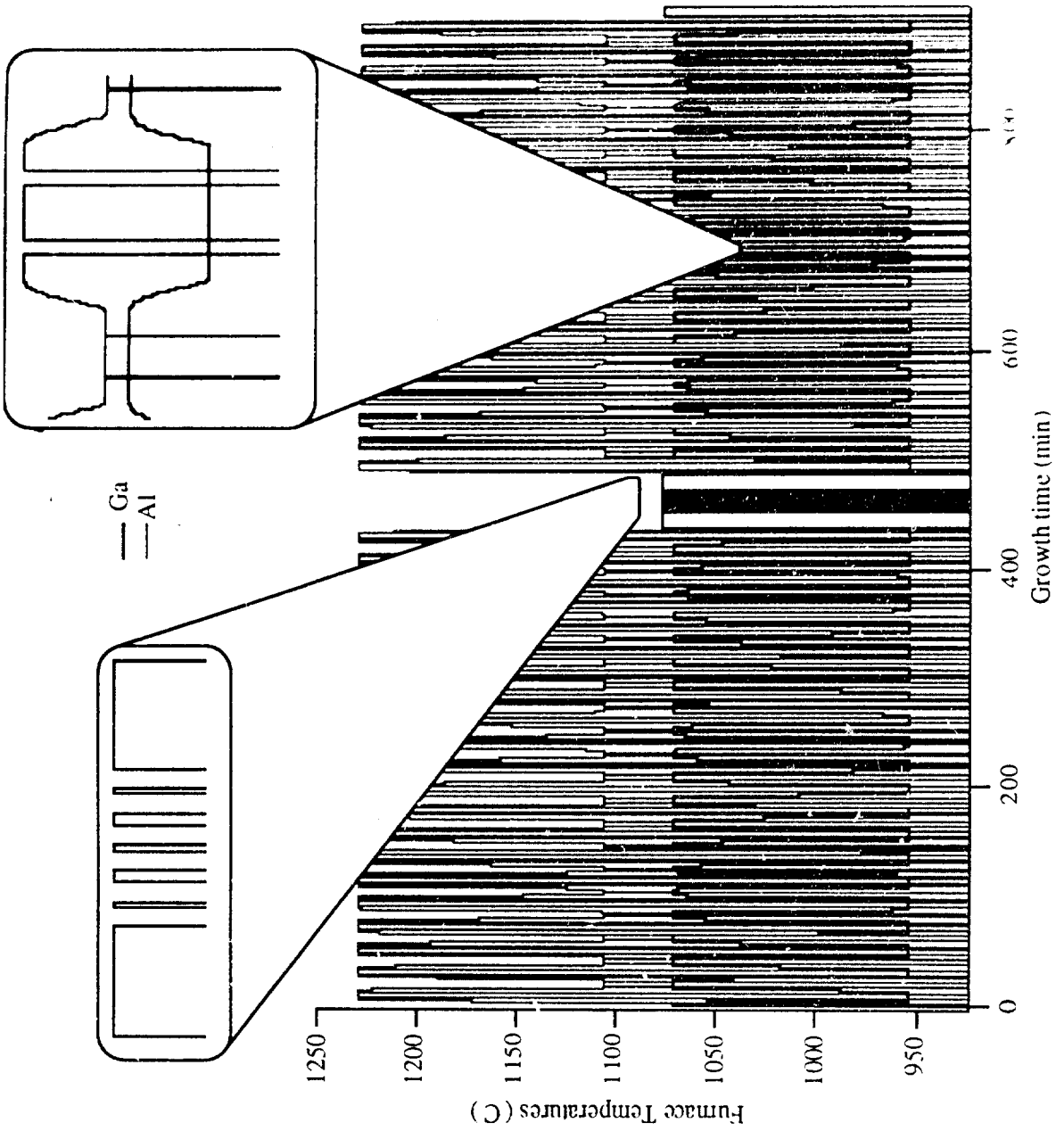
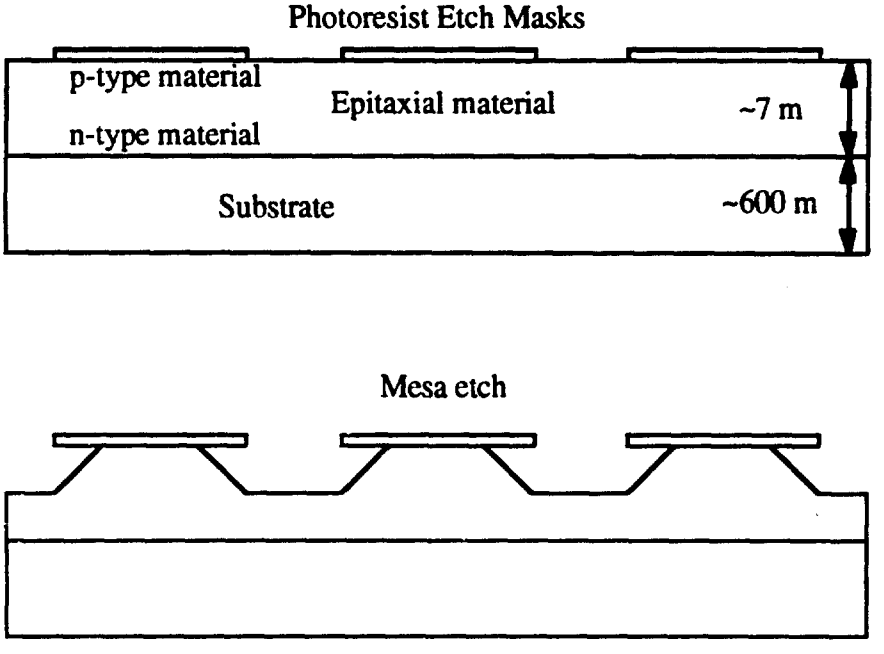


Figure 7 Temperature versus time for the Ga and Al furnaces for the graded cosinusoidally graded composition interface mirror VCSEL. Blown up regions show detail of the Ga growth interruptions surrounding the quantum wells at the left. Detail at the right shows grading of GA and Al temperatures, and growth interruptions of Al during thin GaAs smoothing layer deposition.

A temperature change of 1 degree over 3 to 5 seconds is the fastest change to maintain thermal equilibrium and avoid temperature controller instabilities. Attempts at faster temperature changes would result in thermal lag between the thermocouple temperature and the actual temperature of the group III elements because there is significant thermal resistance between the thermocouple and the melt. For the graded composition profiles used in this study, this limit to rate of temperature change established an upper limit to the growth rate of 0.5 m/hour during graded regions. This rate is comparable to what is used for other III-V device growth, but results in total growth time of approximately 12 hours each for these VCSELs which makes these wafers 3-4 times more expensive to produce than lateral cavity lasers.

3.4 VCSEL Fabrication Process

The complete process for fabrication of the VCSELs is documented in Appendix I. The steps described below are summarized in Figure 8. Photolithography is used to define the VCSEL mesa, and dummy mesas are used to planarize the ohmic contacts.



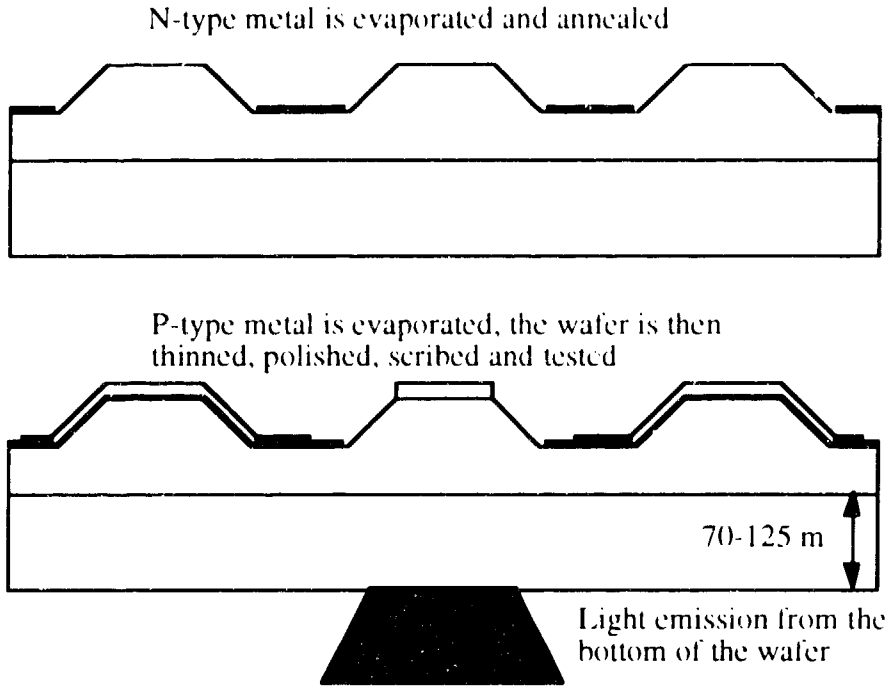


Figure 8 Schematic of process sequence for fabrication of VCSELs

The laser diameter is determined by the area of the p contact metallization. A SEM photo of the top and side views of the completed VCSEL is seen in Figure 9.

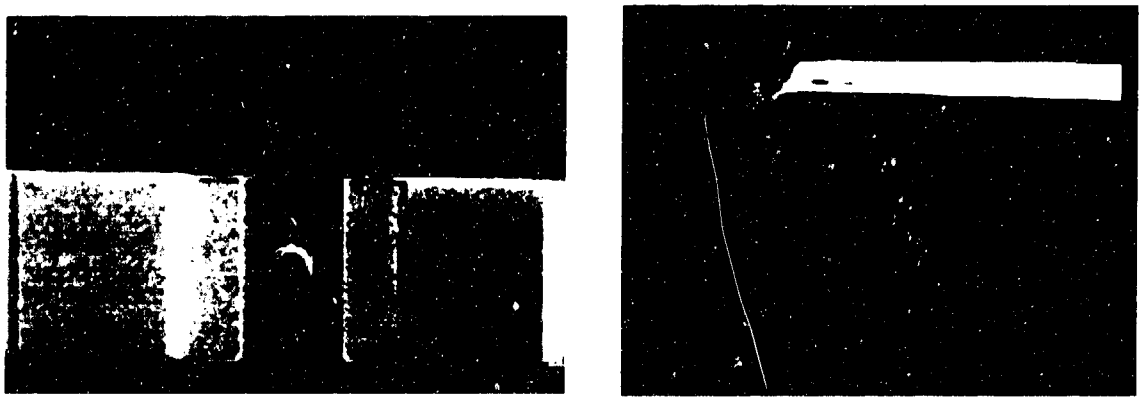


Figure 9 SEM top and side view of completed VCSEL. The metallizations are planarized and laid out to be compatible with both on-wafer high speed probing or high speed interconnection when flip chip mounted to a diamond package.

3.5 Laser Array Design

The VCSELs are fabricated in a process described above into a 4x4 array for compatibility with Rome Laboratory LED optical interconnect demonstration systems. The pitch (laser to laser spacing) is 0.2mm. A scanning electron microscope (SEM)-micrograph of the completed 4x4 array is seen in figure 10.

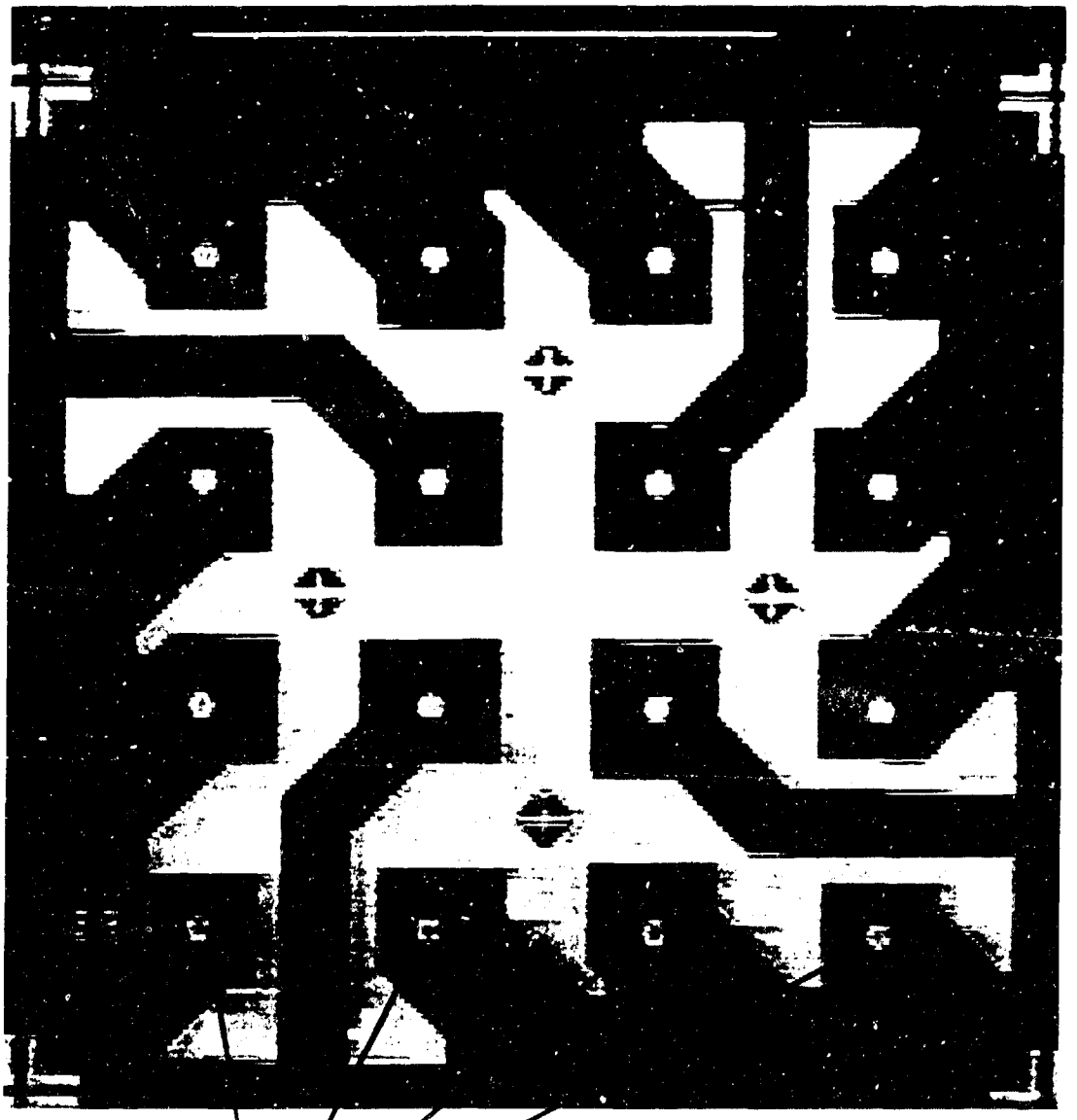


Figure 10 SEM Photomicrograph of VCSEL Array

The 16 lasers are easily visible and the pattern is dominated by the shared ground plane. The layout presents low parasitic inductance and capacitance connections for high speed on wafer probing using co-planar waveguide (CPW) probes for testing prior to packaging. The ohmic contacts to both the n- and p- regions are at the same plane. This layout is dimensionally compatible with the flip-chip diamond heat sink designed for high speed signals described below.

3.6 Diamond Heat Sink Design for High Speed Packaging

Diamond has been chosen for a heat sink/package for the 4x4 laser array for two reasons. First, the thermal conductivity of diamond is the highest for any insulating material. Heat will be extracted from the flip-chip GaAs based VCSELs far better than through a GaAs substrate as in the case of bonding the substrate to a heat sink.[14] Second, diamond exhibits high resistivity which is required for high speed transmission lines. The actual microwave performance of the transmission lines is discussed in the results section. Photographs taken at Rome Laboratories of the diamond heat sink and a 4x4 laser array are seen in Figure 11.

[14]The thermal conductivity of diamond is 10 to 20 W/cm K compared to approximately 0.5W/cm K for GaAs.

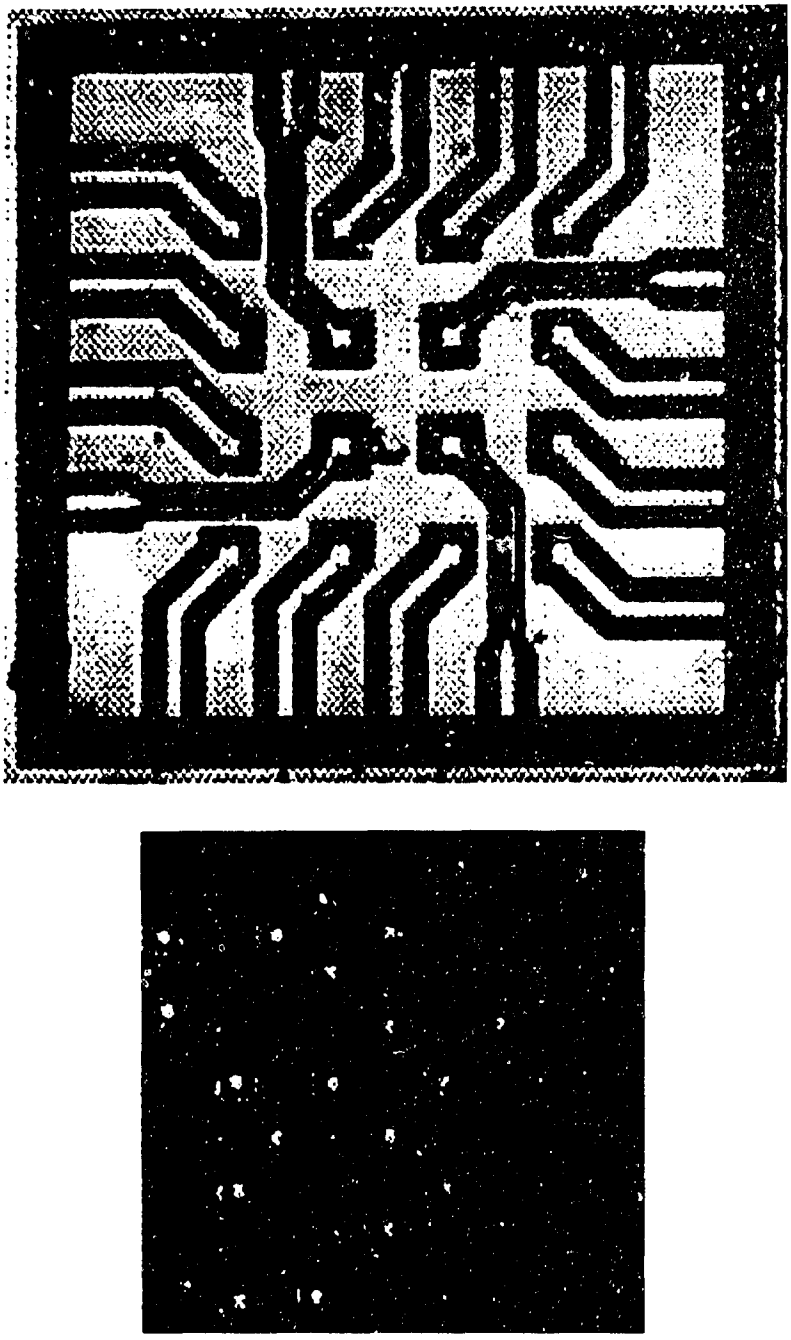


Figure 11 Images of diamond heat sink (above) and 4x4 VCSEL array (below)

3.7 Flip-chip Packaging

In order to mount the 4x4 laser array chip on the diamond heat sink package, it must be flipped upside down so that the contact metallizations which are on the top of the chip can be soldered to the metallization on the heat sink. This process is called flip-chip packaging. Besides providing a better heat sink than the right-side-up mounting, light now comes out of the top of the package through the substrate. This geometry is superior to bringing light out through the metallized side of the VCSEL using a ring/semi-transparent contact because a better ohmic contact can be made to the layer over the entire p-layer surface when using flip-chip mount.

The flip-chip mounting of the VCSEL array demonstrates clear theoretical advantages described above. The technology of this

process, however, is significantly more challenging than conventional substrate down-side mounting of lateral cavity lasers for high speed applications. There are three areas of difficulty with flip-chip packaging of VCSELs. The first is choice of metals for soldering and metals compatible with solder for ohmic contacts. The second problem is metal patterning on the small diamond package using photolithography. The last difficulty is handling and aligning the flip-chip to the diamond package.

A primary requirement for a choice of metal to solder the VCSEL to the diamond heat sink is low melting temperature. It is presumed that the VCSEL performance would be degraded by raising its temperature to very high values during soldering. High temperatures also increase stresses associated with differences in thermal expansion coefficients between metals and the VCSEL material which can be another source of VCSEL performance degradation. An obvious choice for a low temperature solder is indium which melts at 156.7 C.

The use of In introduces another problem with VCSEL soldering. Liquid In readily dissolves the Au metal on top the Ti/Au p-layer ohmic contact. The thin Ti layer may also be vulnerable to the liquid In/Au mixture above it during soldering. Destruction of the Ti layer would likely increase the ohmic contact resistance, and probably change the overall mirror reflectivity (mirror=20 layer stack + GaAs + Ti/Au) enough to degrade the performance of the VCSEL. A proposed solution to this problem is to electroplate 2-5 m of Au on top of the Ti/Au contact prior to soldering. This may be enough sacrificial metal to prevent the In from dissolving all the way to the VCSEL p-contact during soldering.

Another problem with solder is getting a solder film to adhere to the diamond. This problem is solved through using sputter deposition of metal onto the diamond. The starting metal with good adhesion can then be made much thicker through electroplating of In. This approach requires using very thick photoresists (the plating solution dissolves photoresist), or addition of an alternative mask such as polyimide. An alternative technique to plating is direct evaporation of In. An evaporator for In was located in the Materials Science Center at Cornell.

In addition to investigation of pure In, different In alloys were investigated for their suitability as solders which are compatible with the VCSEL metals. A range of In alloy solders from the broad range available from the Indium Corporation of America (Utica , NY) were evaluated. Some alloys were avoided for suspected incompatibility with the application of soldering to a p-type ohmic. For example, In/Sn alloys were attractive as solders with low melting points, but the short- or long-term diffusion of tin (a donor in GaAs) into the p-type contact was feared.These solders may still be employed in the future, but careful study will be required.

4) Results

There were two types of lasers fabricated - those with abrupt interface or graded interface Bragg reflectors. During each round of experiments, both were grown for comparison. In the early growth experiments, there were no working VCSELs. It was discovered from reflectance characterization that the gain region was slightly too thick compared to the desired thickness. Reflectivity of the mirrors also indicated that the growth rate of GaAs was slightly too high. It is presumed that the Ga growth rates is changing during growth due to some uncontrolled variation in the Ga temperature. The cause may be the controller or change in any of the cold junctions between the thermocouple and the controller.

Because the thicknesses of the GaAs and $Al_{0.1}Ga_{0.9}As$ layers were approximately 2% too thick, there was no lasing from VCSELs observed in the early growths. One other important early observation was the difference in voltage drop seen in these devices. The abrupt interface devices had turn-on voltages greater than 20 (voltage at 10 mA), while the graded interface VCSELs had 4 Volt drops at low currents. Clearly the graded interface mirrors reduced diode series resistance. No working abrupt interface VCSELs were ever made. In later experiments, only graded interface VCSELs were studied.

4.1 Lateral Laser Characterization of VCSEL Wafer

An early qualification of the VCSEL wafers was fabrication of simple lateral cavity lasers to test the quality of the material. If there was some unanticipated problem with growth of the MQW gain region of the VCSEL wafers which caused significant non-radiative recombination, this problem could be discovered prior to the more elaborate processing required to make VCSELs.

The PI characteristic from a lateral cavity laser fabricated from a VCSEL laser wafer is seen in Figure 12. A threshold current density of 450 A/cm^2 is indicated. This value is quite good and indicates high quality material. For these long cavity lengths, it would be expected that the threshold density for the 3QW gain region would be approximately 3 times the value for a single QW. This data indicates that an equivalent SQW threshold density of $150A/cm^2$ was obtained. This is as good as the best SQW laser made at Cornell to date. This is somewhat remarkable given that the multilayer reflector is not an optimized design for lateral cavity laser clad layer application. The relatively narrow 20 m cavity width would not be expected to yield threshold current densities as low as those measured for broad area devices, yet these threshold current densities are very low. The conclusion from this study is that the laser material exhibits very high radiative recombination efficiency and should be a high quality gain region for application to VCSELs.

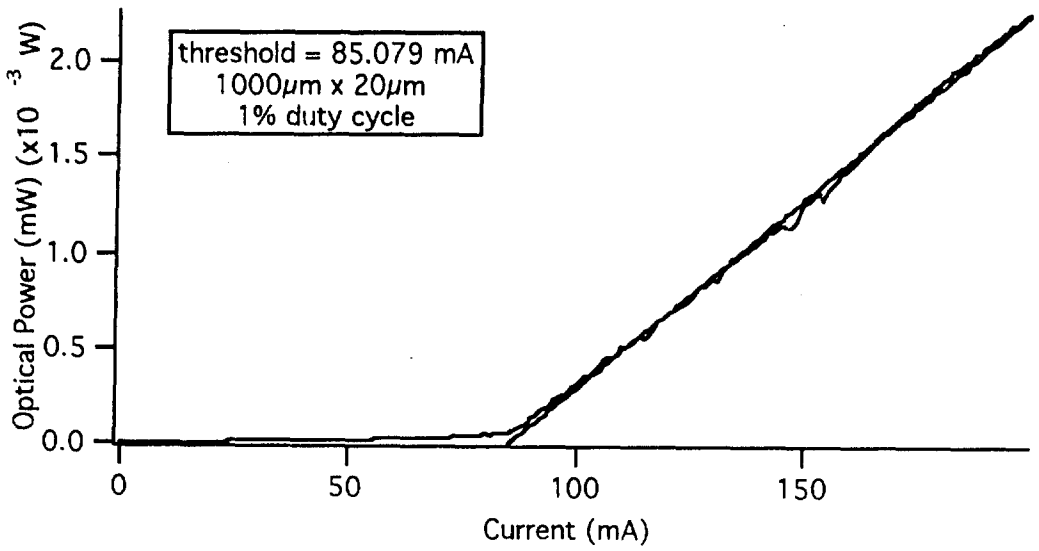


Figure 12 Measured Optical Power versus Current (PI) for a lateral cavity laser fabricated from a graded interface VCSEL wafer

4.2 VCSEL Reflectivity Spectrum

Reflectivity of the wafer with the graded interface reflectors is seen in Figure 13. The agreement between theory and experiment is reasonably good. However, the dip in the reflection corresponding to the gain region at 1040nm is not in the optimum position. A minium at 1060nm, or slightly longer, wold be desirable for CW operation at high current levels where the VCSEL temperature would rise.

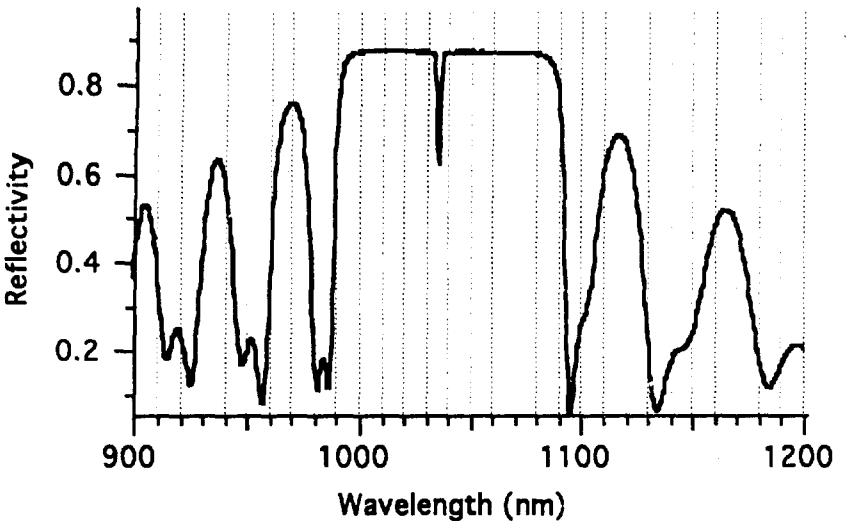


Figure 13 Measured reflectivity at normal incidence as function of wavelength for graded interface mirror VCSEL wafer

4.3 Pulsed IV and Optical Output Power Characteristics

Pulsed IV and optical output characteristics for the graded interface VCSEL are seen in Figure 14. The data is taken for a 1 sec pulse at 1% duty cycle. All data was taken at the Photonics Center at Rome Laboratories. The optical power was measured at the output of an optical fiber. This power is more than 100 times greater than the power from an LED used in other programs aimed at vertical optical interconnects.

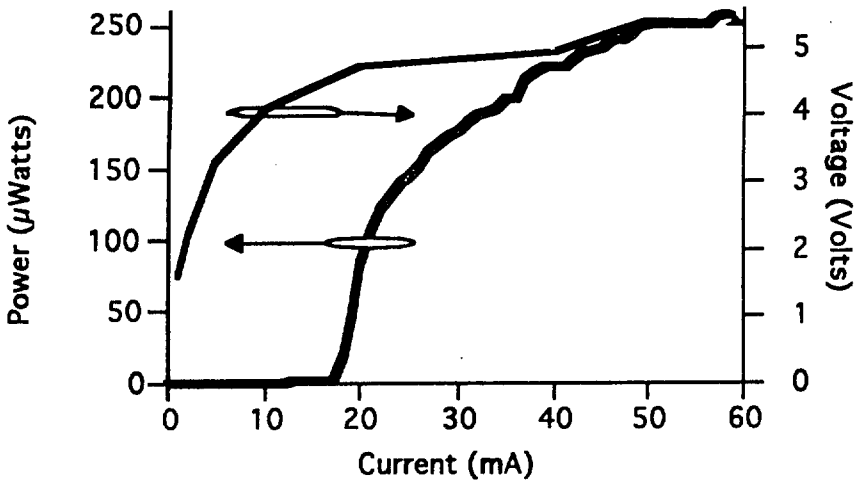


Figure 14 Current-Voltage (IV) and Power-current (PI) characteristics of graded interface VCSEL

4.4 Optical Spectra

The optical spectrum for the VCSEL taken at 1 sec pulse width, 1% duty cycle is seen in Figure 15. Single mode emission at 1.06 m with very good spectral purity is seen. There are no Fabry-Perot modes seen to surround the output because the optical cavity is so short that the spacing of these modes is outside of the gain/reflectivity bandpass for the VCSEL.

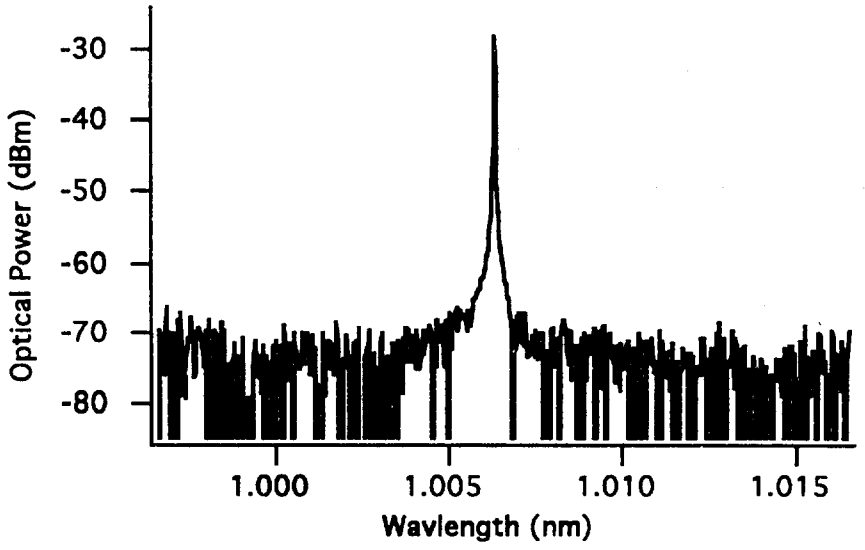


Figure 15 Optical output spectrum of graded interface VCSEL

An optical spectrum for the first graded interface VCSEL grown for this program, which did not perform well is seen in Figure 16. As current is increased, optical output becomes stronger at shorter wavelengths which indicates recombination at higher energy than the minimum energy confined state. This behavior is interpreted as an indication that the peak in gain is at a shorter wavelength than intended due to approximately 1.5% discrepancy between intended and actual Ga growth rates.

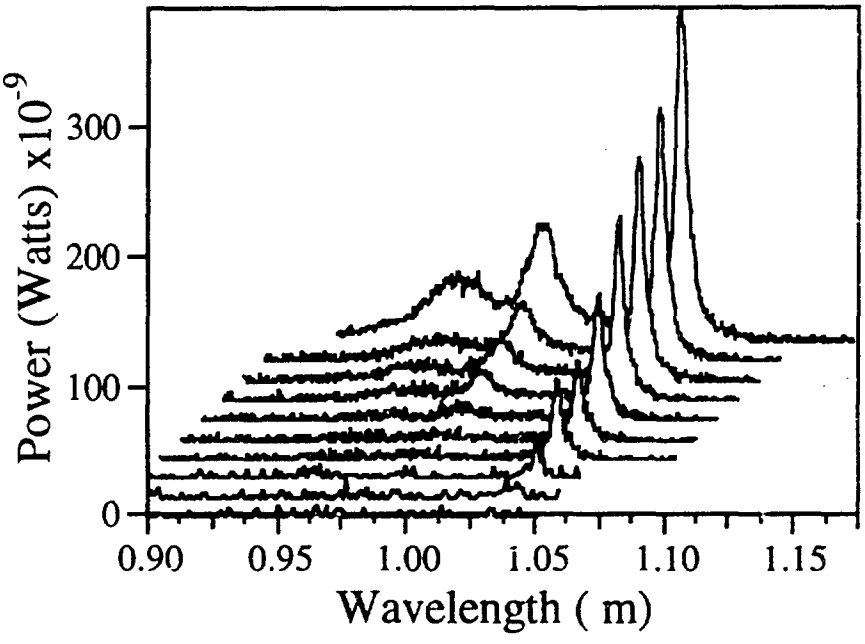


Figure 16 Optical output power spectrum from the first grown VCSEL wafer at increasing bias current levels. Short wavelength emission increases with bias current

It is not clear what transition these higher energy peaks correspond to. They are not different Fabry-Perot modes as the spacing is too close in wavelength for such a short optical cavity. They seem to be too close in energy to the minimum energy emission to be n=2 transitions. Note that when the growth rates are adjusted to insure agreement between designed and observed thicknesses, there is no evidence of these higher energy emissions.

4.5 RF Characterization of Diamond Heat Sink Package

An important concern when using a good thermal conductor for a heat sink and package is any parasitic contribution it might make to high frequency signal losses. For example, a simple solution to heat removal might be to use a semiconductor with better thermal properties, such as Si which would lend itself to easy processing. The parasitic losses at GHz frequencies for Si would be prohibitive due to poor resistivity and relatively high dielectric constant. Even the wide bandgap material, SiC exhibits losses for FET bonding pads which limits high frequency signal applications[15].

Diamond is well known as a good thermal conductor, but no informataion could be found on its application as a substrate for microwave frequency transmission lies. It was expected to show outstanding performance in this application as it has high resistivity and a low dielectric constant.

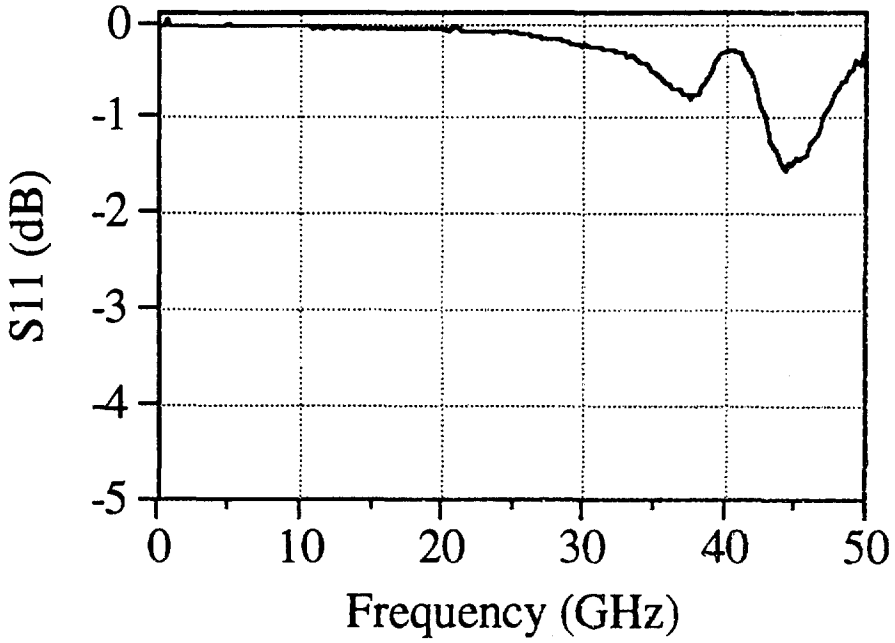


Figure 17 S11 response of transmission lines on CVD diamond heat sink

[15]Cree Research, *Device Research Conference*, Santa Barbara, June, 1993.

Transmission lines were fabricated on CVD diamond and evaluated for application to high speed laser interconnects. The S11 response is seen in Figure 17. This data indicates that parasitic losses associated with the CVD diamond dielectric are very low - much lower than those seen for transmission lines fabricated on GaAs. There will be no RF disadvantage to using the CVD diamond as a high speed package for mounting VCSELs.

The dominant disadvantage to using diamond is the difficulty of processing the very small (1x1mm) pieces which are economical for this application. This problem is the subject of on-going investigation.

5) Publications and Presentations resulting from this research

"Vertical Cavity Surface Emitting Laser Arrays Flip-Chip Mounted onto Microwave Compatible Diamond Heat Sinks", Sean S. O'Keefe, NNF Annual Industrial Affiliates Meeting (Oct. 26-27, 1993).

"Vertical Cavity Surface Emitting Lasers for Flip-Chip Packaged Vertical Optical Interconnects", S.S. O'Keefe, W.J. Schaff, and L.F. Eastman, *Spie's Int. Symp on Optical Engineering in Aerospace Sensing* - Conference **2216** Photonics at the Air Force Photonics Center, Orlando, Fl, April 4-5, 1994

"CPW Transmission Lines on Polycrystalline Diamond Substrates for a 4x4 VCSEL Array", S.S. O'Keefe, G. Martin, D.W. Woodard, W.J. Schaff and L.F. Eastman, *WOCSDICE'94* Cork, Ireland (May 29-June 2, 1994).

6) Appendix I - Processing Log

Processing Sequence for VCSELs

The lithography is done on the GCA 5:1 Stepper in the National Nanofabrication Facility (now the National Nanofabrication Network) at Cornell University. The zero level alignment mark evaporation is done on the CHA evaporator at the National Nanofabrication Facility also. The other metallization steps and the RTA anneal are performed in the lab that is controlled by Prof. Lester Eastman at Cornell University.

1: Zero level alignment marks

Shipley C-20 Primer 4000 RPM
AZ5214 4000 RPM
(~1.1 m thick)
Hot plate bake 90 C 2 minutes
Expose .93 seconds
Hot plate bake 115 C 3 minutes (image reversal)
HTG Flood exposure 60 seconds
Develop in MF321 ~2 minutes

2. Metallization of alignment marks

CHA evaporator
500Å Chrome (Exact thickness is unimportant. It is simply used for visual alignment.)
Acetone soak for liftoff

3. Mesa definition

Dip wafer in NH_4OH:DI :: 1:15 to remove surface oxide and blow dry
Shipley C-20 Primer 4000 RPM
Shipley 812 4000 RPM
(~1.2 m thick)
Hot plate bake 115 C 1 minute

expose 0.37 seconds

Develop in MF321 ~2 minutes

4. Mesa Etch

Mix a solution of 3:1:20 :: H_3PO_4:H_2O_2:H_2O

This will etch GaAs and AlGaAs at a rate of 1600-2000Å/min

Etch the wafers ~3.8 m deep. This depth will place you through the active region and leave you in the n-type material.

Try to stop the etching on GaAs and not AlGaAs in order to obtain a better ohmic contact.

The AlGaAs will look rough (or less reflective) because of the aluminum oxide that forms during the etching.

Remove photoresist in acetone when done.

5. n-Type metallization definition

Shipley C-20 Primer 4000 RPM

Shipley 1400-37 4000 RPM

(~2.7 m thick)

Hot plate bake 90 C 2 minutes

Expose 0.45 sec

YES oven image reversal

HTG flood 60 seconds

Develop in MF 321 ~2 - 2-1/2 minutes

Branson Descum

Dip wafer in NH_4OH:DI :: 1:15 to remove surface oxide and blow dry (Do this JUST BEFORE loading into the evaporator)

6. Evaporate

Nickel	100Å
Au/Ge	900Å
Silver	1000Å
Gold	1000Å

Soak in acetone for liftoff

7. RTA anneal

   450 C 10 seconds

8. p-Type metallization

   Shipley C-20 Primer 3000 RPM

   Shipley 1650 3000 RPM (ramp slowly from 200RPM up to 3000RPM over ~20 seconds and spin at 3000RPM for about 1 minute)

   (~5.5 m thick)

   Hot plate bake 90 C 1 minute

   Expose 0.7 sec

   YES oven image reversal

   HTG flood 60 seconds

   Develop in MF 321 ~2 - 2-1/2 minutes

   Branson Descum

   Dip wafer in NH_4OH:DI :: 1:15 to remove surface oxide and blow dry (Do this JUST BEFORE loading into the evaporator)

9. p-type metal evaporation

Titanium	250Å
Platinum	200Å
Gold	2100Å
Silver	5000Å
Gold	4000Å

   Acetone soak for liftoff

10. Lap and polish wafers to 3-5 mils thickness

11. Scribe into arrays and bars

12. Test

13. Continue with diamond heat sink packaging process

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